IV. Amendments to the Drawings

A substitute drawing sheet 4/5 has been submitted amending FIG. 3B. Specifically, references "262" have been changed to "272" and references "264" have been changed to "274".

V. Remarks

A. Objection to the Specification

The Examiner objects to the Abstract stating that "comprises" should be "includes." It is respectfully submitted that this objection is misplaced. The MPEP may prohibit use of legalistic words such as "whereby" or "said," but "comprise" is not understood to be one of these legalistic words. Nevertheless, the Abstract has been amended as suggested by the Examiner with the understanding that "comprise" and "include" are commensurate in scope.

B. Objection to the Drawings

The Action objects to the drawings because reference character "216" has been used to designate both a "conductive trace" and a "connection" on Pages 8 and 9, Lines 28 and 8, respectively. On Page 8, the specification described MOS device 200 as including "a conductive trace 216 for providing **electrical connection to the gate** 202." (emphasis added) Page 9, Line 8 provides that "each of **connections 216**, 218, 220 **to the corresponding gate**, drain and source regions comprises a metal." It is submitted that reference 216 refers to a connection to the gate and has been used consistently in the two sections of the specification cited by the Examiner, as emphasized by the bolded sections set forth above. Reconsideration and withdrawal of the objection are respectfully requested.

The Action also objects to the drawings for the use of character 262 to designate both the thin oxide layer and the metal interconnection layer. Applicants are grateful to the Examiner for the careful review of the application. A substitute drawing sheet No. 4 amending FIG. 3B and a corresponding amendment to the Specification have been made amending "262" when used for the metal interconnection of FIG. 3B to "272." Accordingly, reconsideration and withdrawal of the objection are respectfully requested.

The Action also objects to the drawings for the use of character 264 to designate both the field oxide region and the metal contact. A substitute drawing sheet No. 4 amending FIG. 3B and a corresponding amendment to the Specification have been made amending "264" when

used for the metal contact of FIG. 3B to "274." Accordingly, reconsideration and withdrawal of the objection are respectfully requested.

C. Rejection under 35 U.S.C. §102

The Action rejects Claims 1-2, 11, 13-14, 17 and 21-22 as being anticipated by U.S. Patent No. 6,268,633 to Pio et al. Reconsideration and withdrawal of this rejection are respectfully requested in view of the following arguments.

First with respect to Claim 1, Claim 1 is directed to an MOS device including first and second/source drain regions (e.g., two implant regions corresponding to the source and drain of an MOS device) with a gate structure formed at least partially between the first and second source/drain regions. A dimension of the gate, defined substantially parallel to at least one of the first and second source/drain regions, "is confined to be substantially within the active region of the device." The MOS device also includes "an isolation structure . . . configured to substantially isolate one or more portions of the first source/drain regions from corresponding portions of the second source/drain regions." It is submitted that Pio et al. does not teach the recited gate or isolation structures.

As explained in connection with prior art FIG. 2C of the present application, "the gate 256 of traditional MOS device 250 extends beyond the active region of the device and onto the field oxide regions 264 (inactive region) of the device." This extended structure detrimentally can cause increased extrinsic gate capacitance and increased gate resistance. By confining the gate structure as claimed, this extrinsic gate capacitance and gate resistance are reduced or eliminated. (See, Application Specification, p.p. 6-7).

In the rejection, the Examiner concludes that gate 4 is "confined to be substantially within the active region of the device." The Examiner does not cite to a specific figure of Pio et al. It is submitted that only FIG. 1 of Pio et al., which is a top plan view of semiconductor substrate 1, can truly illustrate whether the gate 4 of Pio et al is confined as claimed. The field oxide region (and thus inactive region) of Pio et al. is designated by reference 12. (See, e.g.,

FIG. 3.). The field oxide region is not specifically labeled in the top plan view of FIG. 1, but FIGS. 2 and 8-22 clearly show that the longitudinal edges of the source/drain implants 6,7 of the device (which includes gate 4) are defined by the field oxide region 12. It is believed that the length (i.e., the end edges) of source drain regions 6, 7 (as shown in the top plan view of FIG. 1) would also be defined by the field oxide region. In essence, referring to the top plan view of FIG. 1, the active region would be the generally rectangular regions 6 and 7 and the area under gate 4 that connects regions 6 and 7. All other regions of substrate 1 (except for other active regions such as device 3) would be covered by the field oxide and be "inactive", including the significant portions of the end of rectangular gate 4 that extend beyond regions 6 and 7 of FIG. 1. Therefore, it is submitted that the gate 4 of Pio et al. is not "confined to be substantially within the active region of the device" in the dimension of the gate defined substantially parallel to at least one of the first and second source/drain regions as claimed in Claim 1.

Initially, with respect to the "isolation structure" feature of Claim 1, Applicants would like to bring to the Examiner's attention the naming convention "source/drain regions" used in the application. The application provides the following:

> It is to be appreciated that, in the case of a simple MOS device, because the MOS device is symmetrical in nature, and thus bidirectional, the assignment of source and drain designations in the MOS device is essentially arbitrary. Therefore, the source and drain regions may be referred to generally as first and second source/drain regions, respectively, where "source/drain" in this context denotes a source region or a drain region. In a LDMOS device, which is generally not bidirectional, such source and drain designations may not be arbitrarily assigned.

Page 4, second full paragraph. Therefore, when Claim 1 recites that the MOS device includes "first and second source/drain regions" it recites a first source or drain region and a second source or drain region, i.e., two implant regions, not two pairs of implant regions.

As noted above, Claim 1 recites that the MOS device (i.e., an individual transistor device) includes an isolation structure configured to isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain region. The first source/drain region and second source/drain region **are clearly claimed as part of the same MOS device** (i.e., they are claimed as being part of the same "active region" in Claim 1). The Examiner cites to field oxide 12 of FIGS. 1-3 as the claimed isolation structure and argues that the field oxide 12 isolates one or more portions of source/drain 6, 7 (of the first device 2) from one or more portions of the source/drain regions 8,9 (of the second device 3). As is convention, field oxide 12 is formed over substrate 1 of Pio et al. to isolate individual active regions and thus to isolate individual transistor devices, such as high voltage transistor 2 and low voltage transistor 3. Field oxide 12 is **not**, however, formed such that it isolates portions of the source and drain regions of the same MOS device. As previously stated, the claimed first source/drain region and second source/drain region are clearly part of the same MOS device. Thus, the isolation region identified by the Examiner, which isolates individual devices and not regions within the same device is not "an isolation structure . . . configured to substantially isolate one or more portions of the first source/drain region from corresponding portions or the second source/drain region."

For at least these reasons (i.e., that Pio et al. does not recite the claimed gate and isolation region features), Claim 1 is not anticipated by and is allowable over the art of record. Claims 2-13 depend from independent Claim 1 and are, therefore, also allowable for at the least the reasons set forth for Claim 1.

Independent Claim 14 is directed to a method of forming a MOS device. The method recites the formation of substantially confined gate and isolation structures analyzed above in connection with Claim 1. For at least these reasons, Claim 14 and Claims 15-20, which depend from Claim 14, are also allowable over the art of record.

Last, Independent Claim 21 is directed to an integrated circuit including at least one MOS device where the MOS device including the substantially confined gate and isolation structures

analyzed above in connection with Claim. It is submitted that Claim 21 and Claims 22-23, which depend from Claim 21, are allowable over the art of record.

Reconsideration and withdrawal of the anticipation rejections are respectfully requested.

D. Rejection under 35 U.S.C. §103

The Action rejects Claims 3-10, 12, 15-16, 18 and 20 as being obvious in view of Pio et al. and several other references. These claims depend from independent Claims 1, 14 and 21. As set forth above, these claims are allowable for at least the reasons argued for independent Claims 1, 14 and 21.

Reconsideration and withdrawal of the rejections of these claims are respectfully requested.

VI. Conclusion

In view of the foregoing remarks and amendments, Applicant(s) submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

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Joseph A. Powers, Reg. No.: 47,006
Attorney For Applicant(s)

DUANE MORRIS LLP
One Liberty Place
Philadelphia, Pennsylvania 19103-7396
(215) 979-1842 (Telephone)
(215) 979-1020 (Fax)